High-Order CIFB Delta-Sigma Modulator with High OSR

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ABSTRACT

This paper presents tenth-order delta-sigma modulator for 3-bit quantizer with cascade of integrator with multiple feedback (CRFB). The quantization noise suppression is optimized by increasing out-of-band gain (OBG) of the modulator to 6. The modulator signal-to-noise transfer function (STF) and noise transfer function (NTF) are discussed. The NTF zero optimization technique is applied to suppress quantization in the signal band to suppress quantization noise. The CIFB topology allows to utilize multiple feedback digital-to-analog converter (DAC) for higher stability of the modulator. Due to the CIFB topology the STF shows flat response rather than peak in case CIFF. The 0.5-V full scale of the modulator optimized to maximize the signal-to-noise ratio (SNR). The oversampling ratio of the modulator selected to 128 to get smaller bandwidth advantage with higher SNR of 189-dB with ideal model. The out-of-band Gain (OBG) of the modulator optimized for higher performance. The higher values of the OBG also investigated for high-order modulator. Due to minimum value of OBG also investigated for better performance.

Keywords: Signal transfer function, DC Gain, Multi-Bit Delta-Sigma, Noise transfer function, Operational amplifier.

1. INTRODUCTION

A high-order modulator investigate for multi-bit quantization. The modeling and simulation show the tenth-order modulator can achieve SNR of 189 dB. The OBG of 2.5 with OSR of 128 with without NTF zero optimization technique. Many of the practical parameters like temperature, pressure sensors or transducer output are very small. The complete modulator circuit non-idealities further simulated like limited DC gain, limited slew-rate, thermal noise, and flicker noise. It is required to amplify these signals with very high and then required to digitized. It requires very high accuracy analog-to-digital converter (ADC). A 24-bit noise shaping modulator is modeled and simulated for moderate to smaller bandwidth application. The modulator performance parameters like full-scale and OBG varied to enhance the performance of the modulator. The power consumption is one of the main constraints of sensory systems with very small output signals produced by sensors constraints quite high demands on the power consumption of the interface circuits processing small signals. In high resolution

switched capacitor systems with small inputs, for a given sampling capacitor size, a large oversampling ratio (OSR) is typically required to lower the thermal noise level below the accuracy requirement of the system, and this leads to an increased operational transconductance amplifier (OTA) power consumption. Even though technology scaling has considerably reduced the digital power in sensory systems, analog front-end circuits including the ADCs have not benefited from scaling in terms of power dissipation [1]-[3]. A 24-bit modulator design is proposed with chopping technique. The proposed design presents a low-power high-precision delta-sigma ADC mainly used for DC measurement, especially in applications with high input impedance. The design uses the 3rd order modulator with signle-bit quantizer. The design starts from modeling the design and finding the coefficient and getting an estimate of the performance of the modulator. The estimated performance of the modulator will be used as initial value that may degrade and result in much lower performance. Also the configurable chopping scheme is proposed to reduce the input-dependent residual offset caused by the clock feed-through. Furthermore, it also improves noise performance in the first integrator. The delay generation for the chopping techniques to adjust the delay cell timing. The digital control logic will generate the logic for these delay cells. The 1.17 mm^2 chip is fabricated in a standard 65 nm CMOS process. Measurement results show that the ADC achieves 20-bit resolution, 10 ppm INL and a 0.6 μV offset, while consuming 860 μW from 3.3 V supply. It also overcomes the residual offset caused by clock feedthrough, as well as the mismatch in the first integrator. A configurable delay cells is employed to reduce the chopping spikes. At the same time, an additional chopper is applied to cancel the mismatch of the integrator. [4]. A 20-bit incremental ADC for battery-powered sensor applications is presented. It is based on an energy-efficient zoom ADC architecture, which employs a course 6-bit SAR conversion followed by a fine 15-bit ΔΣ conversion. To further improve its energy efficiency, the ADC employs integrators based on cascoded dynamic inverters for extra gain and PVT tolerance. Dynamic error correction techniques such as auto-zeroing, chopping and dynamic element matching are used to achieve both low offset and high linearity. Measurements show that the ADC achieves 20-bit resolution, 6 ppm INL and 1 μV offset in a conversion time of 40 ms, while drawing only 3.5 μA current from a 1.8 V supply. This corresponds to a state-of-the-art figure-of-merit (FoM) of 182.7 dB. The 0.35 mm 2 chip was fabricated in a standard 0.16 μm CMOS process [5]. Another work describes a second-order incremental converter based on a second order delta-sigma modulator. The scheme uses a 3-bit DAC with inherent linearity, an optimal reset of integrators, and gives rise to an effective offset cancellation with a novel technique based on single or double chopping. The circuit, fabricated in a mixed 0.18-0.6 μm CMOS technology, obtains 1.5-μV residual offset with $2V_{PP}$ fully differential range. The measured resolution is 19-bit obtained with 512 clock periods [6]. Another incremental ADC described as a low-power 22-bit incremental ADC, including an on-chip digital filter and a low-noise/low-drift oscillator, realized in a 0.6-μm CMOS process. It incorporates a novel offset-cancellation scheme based on fractal sequences, a novel high-accuracy gain control circuit, and a novel reduced-complexity realization for the on-chip sinc filter. The measured output noise was 0.25 ppm (2.5 V_{RMS}), the DC offset 2 μV, the gain error 2 ppm, and the INL 4 ppm. The proposed design with measurement results operates with a single 2.7–5 V supply and draws only 120 μA current during conversion [7].

This paper proposed presents tenth-order delta-sigma modulator for 3-bit quantizer with cascade of integrator with multiple feedback (CRFB). The quantization noise suppression is optimized by increasing out-of-band gain (OBG) of the modulator to 6. The modulator signal-to-noise transfer function (STF) and noise transfer function (NTF) are discussed. The NTF zero optimization technique is applied to suppress quantization in the signal band to suppress quantization noise. The CIFB topology allows to utilize multiple feedback digital-to-analog converter (DAC) for higher stability of the modulator. Due to the CIFB topology the STF shows flat response rather than peak in case CIFF. The 0.5-V full scale of the modulator optimized to maximize the signal-to-noise ratio (SNR). The oversampling ratio of the modulator selected to 128 to get smaller bandwidth advantage with higher SNR of 189-dB with ideal model. The out-of-band Gain (OBG) of the modulator optimized for higher performance. The higher values of the OBG also investigated for high-order modulator. Due to minimum value of OBG also investigated for better performance.

After the introduction, the second section discuss the design of the modulator design with CIFB and CIFF structure, while the third section describes the modeling and simulation of the modulator and explain the operational amplifier for integrator for the nine-order with 4-bit quantizer for switched-capacitor implementation. Finally, the section four concludes the paper.

2. MODULATOR DESIGN

The design of delta-sigma modulator initiated using modeling of the modulator [8]-[9]. A higher order with nine integrators in the loopfilter and four-bit quantizer modulator modeled using Delta-Sigma Toolbox [10]. The cascade of integrator with multiple feedforward (CIFB) as well as cascade of integrators with multiple feedback (CIFB) investigate for higher out-of-band-gain (OBG) of 6 with moderate oversampling ratio of 64 without NTF zero optimization technique. The modulator with CIFB topology can achieve SNR of 148 dB with OSR of 64. Due to the reason of low pass modulator, the STF of the modulator have low pass behavior. While the NTF have high pass response to shape more quantization noise at high frequency. The coefficients of the proposed 9th order multiple bit CIFB obtained from Delta-Sigma Toolbox is shown in the Table-I. These coefficients represent the ratio of capacitors at the discrete-time implementation of the modulator. While for the CT implementation these coefficient needs to be converted into the CT equivalent coefficient [9]. Then these converted coefficients will be used to choose the resistor and capacitor ratio considering the sampling frequency. Those coefficients which are not mentioned, have value zero. The signal-transfer function (STF) and noise transfer function (NTF) of the modulator is shown in Figure 1. As it is shown from the Figure 1 clearly that the OBG of the CIFB modulator is 6. While STF of the modulator shows low-pass response to allow those signals, which are at low frequencies and attenuate high frequency signal. The Figure 2 shows ideal STF and NTF plot of the CIFB modulator topology. The Figure 3 shows the output power spectral density (PSD) plot with SNR of 148, achieving effective number of bit (ENOB) of 24-bit. The modulator NTF shows a sharp noise shaping response due to the reason that all integrator inside the loopfilter is assumed having infinite DC gain. The noise floor is at the level of

-170dB, the quantization noise is suppressed maximum with nine integrators inside the loop filter. Due to moderate OSR of 64, the signal bandwidth is small. Due to CIFB topology of the modulator the signal swing inside the loopfilter is large as a results operational amplifier with very high DC gain will be demanded for the suppression of the quantization noise. Due to CIFB topology the stability of the loopfilter is very high due to the advantage of multiple feedbacks, while the overall modulator becomes power hungry with many high DC gain amplifier inside the loopfilter.

1. RESULTS & DICUSSION

The complete modulator with coefficient obtained from the Toolbox are simulated further to get an estimate the performance of the modulator. To realize the practical implementation of the modulator, non-idealities needs to be simulated so that circuit designed can get an estimate of the performance. The simulation environment SDToolbox [11] which simulates the circuit non-idealities are used. This section will discuss about the circuit non-idealities like thermal noise or kT/C, flicker noise, finite operational amplifier gain, finite slew-rate, finite gain-bandwidth (GBW).

4. CONCLUSION

A presents tenth-order delta-sigma modulator for 3-bit quantizer with cascade of integrator with multiple feedback (CRFB). The quantization noise suppression is optimized by increasing out-of-band gain (OBG) of the modulator to 6. The modulator signal-to-noise transfer function (STF) and noise transfer function (NTF) are discussed. The NTF zero optimization technique is applied to suppress quantization in the signal band to suppress quantization noise. The CIFB topology allows to utilize multiple feedback digital-to-analog converter (DAC) for higher stability of the modulator. Due to the CIFB topology the STF shows flat response rather than peak in case CIFF. The 0.5-V full scale of the modulator optimized to maximize the signal-to-noise ratio (SNR). The oversampling ratio of the modulator selected to 128 to get smaller bandwidth advantage with higher SNR of 189-dB with ideal model. The out-of-band Gain (OBG) of the modulator optimized for higher performance. The higher values of the OBG also investigated for high-order modulator. Due to minimum value of OBG also investigated for better performance.

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